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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,529	10/06/2000	John D. Logue	X-735 US	1502

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EXAMINER	
ZHENG, EVA Y	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/684,529	LOGUE ET AL.	
	Examiner	Art Unit	
	Eva Yi Zheng	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/13/04,8/16/04. 10/12/04*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 8-10 and 12-22 are rejected under 35 U.S.C. 102(a) as being anticipated by Waizman (IEEE Feb. 1994).

a) Regarding claim 1, Waizman discloses a digital clock manager having a reference input terminal (CLK in Fig. 2), a skew input terminal (XCLK in Fig. 2), an output terminal (V_{CNTL} in Fig. 2), and a frequency adjusted output terminal (output of CLKGEN in Fig. 2), the digital clock manager comprising:

a delay lock loop (DLL)(PHASE ALIGN in Fig.2) coupled to the reference input terminal, the skew input terminal, and the output terminal; and

a digital frequency synthesizer (CLKGEN in Fig. 2) having a variable oscillator (inherent as ring oscillator; last paragraph by Waizman), coupled to the delay lock loop and the frequency adjusted output terminal (as shown in Fig. 2 and more detailed in Fig. 3).

b) Regarding claim 19, Waizman discloses a method to generate an output clock signal and a frequency adjusted clock signal from a reference signal (CLK in Fig. 2), wherein the output clock signal (V_{CNTL} in Fig. 2) is synchronized with the frequency adjusted clock signal (CLK in Fig. 2) during a concurrence; the method comprising:

generating a synchronizing clock signal (V_{CNTL} in Fig. 2);

matching a DLL output delay with a DFS output delay (as shown in Fig. 3);

generating the output clock signal lagging the synchronizing clock signal by the DLL output delay (T_D in Fig. 3 and paragraph 4 by Waizman); and

generating the frequency adjusted clock signal so that an active edge of the frequency adjusted clock signal lags an active edge of the synchronizing clock signal by the DFS output delay during the concurrence (as shown in Fig. 3 and 4).

c) Regarding claim 2, Waizman discloses the digital clock manager of Claim 1, wherein the delay lock loop is configured to generate an output clock signal on the output terminal (CLK in Fig. 2) which synchronizes a reference clock signal on the reference input terminal (CLK in Fig. 2) with a skewed clock signal on the skew input terminal (XCLK in Fig. 2).

d) Regarding claim 3, Waizman discloses the digital clock manager of Claim 1, wherein the digital frequency synthesizer is configured to generate a frequency adjusted clock signal on the frequency adjusted output terminal (CLK in Fig. 2) and wherein the frequency adjusted clock signal is synchronized with the output clock signal (V_{CNTL} in Fig. 2) during concurrences.

e) Regarding claim 4, Waizman discloses the digital clock manager of Claim 1,

wherein the delayed lock loop comprises a DLL output circuit having a DLL output delay (T_D in Fig. 4).

f) Regarding claim 5, Waizman discloses the digital clock manager of Claim 4, wherein the digital frequency synthesizer comprises a DFS output circuit having a DFS output delay (T_D in Fig. 3).

g) Regarding claim 8, Waizman discloses the digital clock manager of Claim 1, wherein the delay lock loop is derives a synchronizing clock signal (V_{CNTL} in Fig. 2) to the digital frequency synthesizer (CLKGEN in Fig. 2).

h) Regarding claim 9, Waizman discloses the digital clock manager of Claim 8, wherein the delay lock loop is configured to generate an output clock signal on the output terminal (CLK in Fig. 4), wherein the output clock signal lags the synchronizing clock signal by a DLL output delay (2 T_D in Fig. 4).

i) Regarding claim 10, Waizman discloses the digital clock manager of Claim 9, wherein the digital frequency synthesizer (as shown in Fig. 3) is configured to generate a frequency adjusted clock signal on the frequency adjusted output terminal (CLK in Fig. 2), wherein an active edge of the frequency adjusted clock signal lags an active edge of the synchronizing clock signal by a DFS output delay during a concurrence period (T_D in Fig. 4).

j) Regarding claim 12, Waizman discloses the digital clock manager of Claim 1, further comprising a variable delay circuit (VCDL in Fig. 3) coupled between the delayed lock loop and the output terminal.

k) Regarding claim 13, Waizman discloses the digital clock manager of Claim 1, further comprising a variable delay circuit (VCDL in Fig. 3) coupled between the digital frequency synthesizer and the frequency adjusted output terminal.

l) Regarding claim 14, Waizman discloses the digital clock manager of Claim 1, further comprising a multiplexer (MUX in Fig. 3) having a first input terminal coupled to the reference input terminal, a second input terminal coupled to the delay lock loop, and an output terminal coupled to the digital frequency synthesizer (as shown in Fig. 2 and 3).

m) Regarding claim 15, Waizman discloses the digital clock manager of Claim 1, wherein the delay lock loop is configured to provide a synchronizing clock signal to the second input terminal of the multiplexer (MUX in Fig. 3).

n) Regarding claim 16, Waizman discloses the digital clock manager of Claim 15, wherein the digital frequency synthesizer (CLKGEN in Fig. 2) is configured to perform a frequency search phase using a reference clock signal (CLK in Fig. 2) provided to the reference input terminal.

o) Regarding claim 17, Waizman discloses the digital clock manager of Claim 16, wherein the digital frequency synthesizer is configured to provide a frequency adjusted clock signal based on the synchronizing clock signal (as shown in Fig. 2).

p) Regarding claim 18, Waizman discloses the digital clock manager of Claim 1, wherein the digital frequency synthesizer performs a frequency search while the delay lock loop is performing lock acquisition (CONTROL in Fig. 3).

q) Regarding claim 20, Waizman discloses the method of Claim 19, wherein the step of matching a DLL output delay with a DFS output delay comprises synchronizing a DLL output circuit with a DFS output circuit (as shown in Fig. 2).

r) Regarding claim 21, Waizman discloses the method of Claim 19, further comprising performing lock acquisition (CONTROL in Fig. 3).

s) Regarding claim 22, Waizman discloses method of Claim 21, further comprising the performing a frequency search during lock acquisition (CONTROL in Fig. 3).

3. Claims 1, 2 and 4-11 are rejected under 35 U.S.C. 102(e) as being unpatentable by Hassoun (US 6,487,648 B1).

a) Regarding claim 1, as shown in Figure 4, Hassoun discloses a digital clock manager having a reference input terminal (REF_CLK), a skew input terminal (CLK_FB), an output terminal (O_CLK), and a frequency adjusted output terminal (CLK_J), the digital clock manager comprising:

a delay lock loop (DLL) (304B) coupled to the reference input terminal, the skew input terminal, and the output terminal; and

a digital frequency synthesizer (304A) having a variable oscillator (inherent as crystal oscillator, Col 11, L15-20), coupled to the delay lock loop and the frequency adjusted output terminal.

b) Regarding claim 2, Hassoun discloses wherein the delay lock loop is configured to generate an output clock signal on the output terminal, which synchronizes a reference clock signal on the reference input terminal with a skewed clock signal on the skew input terminal. (Col 10, L5-13; Fig. 5)

c) Regarding claim 4, Hassoun discloses wherein the delay lock loop (304B in Fig. 4) comprises a DLL output circuit (510 in Fig 5) having a DLL output delay (D-CLK in Fig. 5).

d) Regarding claim 5, Hassoun discloses wherein the digital frequency synthesizer (304A in Fig. 4) comprises a DFS output circuit (510 in Fig 5) having a DFS output delay (D-CLK in Fig. 5).

e) Regarding claim 6, Hassoun discloses wherein the DLL output delay is substantially equal to the DFS output delay (510 in Fig. 5).

f) Regarding claim 7, Hassoun discloses wherein the DLL output circuit comprises a plurality of components and the DFS output circuit comprises the same components (as shown in Fig. 4 and 5).

g) Regarding claim 8, Hassoun discloses the digital clock manager of Claim 1, wherein the delay lock loop is derives a synchronizing clock signal (O-CLK in Fig. 4) to the digital frequency synthesizer (Clk-j in Fig. 4).

h) Regarding claim 9, Hassoun discloses the digital clock manager of Claim 8, wherein the delay lock loop is configured to generate an output clock signal on the output terminal (O-CLK in Fig. 4), wherein the output clock signal lags the synchronizing clock signal by a DLL output delay (as shown in Fig. 5).

i) Regarding claim 10, Hassoun discloses the digital clock manager of Claim 9, wherein the digital frequency synthesizer (as shown in Fig. 4) is configured to generate a frequency adjusted clock signal on the frequency adjusted output terminal (O-CLK in Fig. 4), wherein an active edge of the frequency adjusted clock signal lags an active

edge of the synchronizing clock signal by a DFS output delay during a concurrence period (as shown in Fig. 8 and 9).

j) Regarding claim 11, Hassoun discloses wherein the DLL output delay is substantially equal to the DFS output delay (510 in Fig. 5).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Yi Zheng whose telephone number is (571) 272-3049. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-879-9306.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Eva Yi Zheng
Examiner
Art Unit 2634

January 25, 2005

SHUWANG LIU
PRIMARY EXAMINER